Novel Current-Scaling Current-Mirror a-Si:H TFT Pixel Electrode Circuit with Cascade Capacitor for AM-OLEDs

Hojin Lee¹, Juhn-Suk Yoo², Chang-Dong Kim², In-Jae Chung², and Jerzy Kanicki¹

¹Organic and Molecular Electronics Laboratory, Department of Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor, Michigan 48109, USA Phone: +1-734-936-0972 Fax: +1-734-615-2843 E-mail: kanicki@eecs.umich.edu ²LG. Philips LCD Research & Development Center, An-Yang, Korea

We proposed the amorphous silicon thin-film transistor (a-Si:H TFT) pixel electrode circuit with current-scaling function that can be used for active-matrix organic light-emitting displays (AM-OLEDs). In contrast to the conventional current-mirror circuit, this circuit with cascaded storage capacitors can provide a high data-to-OLED current ratio without increasing the a-Si:H TFT size. Moreover, since the number of signal line is reduced in the proposed pixel electrode circuit, the pixel layout and the driving scheme can be simplified in comparison to previously reported cascade capacitor circuit.

1. Introduction

Over last several years, it was shown by several authors [1-3] that the current driving pixel electrode circuits are among the most desirable solutions for active-matrix organic lightemitting displays (AM-OLEDs). However, as display size and resolution increase, a large timing delay can be observed at a low data current and its importance increases with the display size [4]. To address this issue, several solutions have been proposed based on polycrystalline silicon (poly-Si) thin-film transistor (TFT) technology such as current-mirror circuit [5, 6] and series-connected TFT circuit [7]. Besides poly-Si TFTs, we also proposed hydrogenated amorphous silicon (a-Si:H) TFT based current-scaling pixel electrode circuit to address this problem [4]. In this paper, we present the improved current driving pixel electrode circuits based on a-Si:H TFT technology with a enhanced current scaling function. A current mirror circuit with a cascaded storage capacitor is proposed here to achieve a high data-to-OLED current ratio without increasing TFT size in comparison with the conventional current mirror pixel circuit. At the same time, by removing one control signal line, this circuit has a much simpler pixel layout and driving scheme than the



Figure 1 Schematic of (a) the cascaded-capacitor current mirror pixel electrode circuit and (b) operational waveforms simulated by HSPICE.

previous cascade capacitor pixel electrode circuit.

2. Operation of the Current-Scaling Pixel Electrode Circuit

The proposed current-driven pixel electrode circuit consists of two switching TFTs (T1 and T2), one mirror TFT (T4), one driving TFT (T3), and two storage capacitors (C_{ST1} , C_{ST2}) connected between a scan line and ground with a cascade structure, Figure 1 (a). The signals of V_{SCAN} , I_{DATA} , and V_{DD} are supplied by the external drivers while the anode of OLED is connected to V_{DD} . In comparison to the cascade capacitor current-scaling pixel electrode circuit reported previously [4], by employing the current mirror TFT structure, the control signal line can be removed to simplify the pixel layout and driving scheme as well as to enable OLED to light up during ON-state even when top anode light-emitting device structure is used.

Here we define I_{OLED-ON} and I_{OLED-OFF} as the current flowing through OLED during the ON- and OFF-state, respectively. $I_{\mbox{\scriptsize OLED-OFF}}$ is also defined as the scaled-down current from $I_{OLED-ON}$ by the ratio of C_{ST2}/C_{ST1} . The pixel circuit operation mechanism can be described as follow: During the ON-state, V_{SCAN} turns on the T1 and T2, and I_{DATA} (= $I_{OLED-ON}$) passes through T1 and T4 as the solid line shown in Fig. 1 (a), and sets up the voltage at T2 drain electrode (node A). At the same time, the voltage at T4 gate electrode (node B) is set by I_{DATA} passing through T4. Since I_{DATA} is current source, the gate voltage of T4 is automatically set high enough to allow the fixed IDATA flowing through T1 and T4. In the pixel simulation, since the current-scaling is not controlled by the geometry ratio of the transistors, T1, T3, and T4 are designed as having the same geometries (W=50µm, and L=4 μ m). The T2 size is set to be the small (W=10 μ m, and L=4µm) to reduce the voltage drop due to the parasitic capacitance when V_{SCAN} turns off. Since in the ideal case T3 and T4 are assumed identical and the gate bias ($V_{B ON}$) is common to both TFTs, the same amount of current (IDATA) is expected to flow through OLED to T3 by V_{DD} . The $V_{B\ ON}$ will be stored in both C_{ST1} and C_{ST2}, and the voltage across



Figure 2 Variation of the simulated $I_{OLED_ON},$ $I_{OLED_OFF},$ and I_{AVE} as a function of I_{DATA} for various C_{ST2}/C_{ST1} ratios.

 C_{ST2} is $V_{SCAN} - V_{B_ON}$.

When the pixel changes from the ON- to the OFF-state, V_{SCAN} turns off T1 and T2. Because C_{ST2} is connected between the scan line and the node B to form a cascade structure with C_{ST1} , the change of V_{SCAN} will reduce V_{B_ON} to V_{B_OFF} due to the feed-through effect of the capacitors. V_{B_OFF} can be derived from the charge conservation theory as $V_{B_OFF} = V_{B_ON} - \Delta V_{SCAN} \cdot C_{ST2} / (C_{ST1} + C_{ST2})$. A reduced T3 gate voltage (V_{B_OFF}) will be hold in C_{ST1} and C_{ST2} and it will continuously turn on T3 during the OFF-state. Since gate bias of T3 (V_{B_ON}) is reduced to V_{B_OFF} by the ratio of cascaded capacitor, a scaled-down data current (I_{OLED_OFF}) will flow through OLED, shown as the dashed line in Fig 1 (a). Consequently, when a very large data current (I_{DATA}) can be used to charge the pixel electrode to shorten the pixel programming time, a smaller driving current (I_{OLED_OFF}) can be achieved for lower gray scales at the same time.

3. Simulated Electrical Properties of the Proposed Pixel Electrode Circuit

The proposed current-scaling pixel electrode circuit was evaluated by H-SPICE and an example of waveforms is shown in Fig 1 (b). In this specific case, in ON-state, the voltage at node B is set to appropriate level to allow IDATA of $1\mu A$ to pass through T3 and T4 while V_{SCAN} and V_{DD} are hold at 30 and 15V, respectively. The time for ON- and OFFstate was set to 0.33 and 33ms, respectively. To investigate the current scaling ratio of the proposed pixel electrode circuit, we changed the I_{DATA} from 0.2 to 5µA and measured the corresponding IOLED ON and IOLED OFF flowing through the diode for different ratios of cascaded-capacitors. In ONstate, the I_{OLED ON} is identical to the data current (I_{DATA}), Fig. 2 (a). When the pixel circuit operates in OFF-state, the diode current (I_{OLED OFF}) is scaled-down by the ratio of cascade capacitor as discussed above and in [4]. From Fig. 2 (b), it is obvious that the larger C_{ST2}/C_{ST1} results in significant decrease of the I_{OLED OFF} at lower I_{DATA}. However, as shown in the figure, too large ratio of C_{ST2}/C_{ST1} (> 1/4) resulted in the saturation of I_{OLED OFF}, which eventually can deteriorate the current scaling function.

Since the OLED current value is different during ON- and OFF-state, we define the average OLED current (I_{AVE}) during one frame time as I_{AVE} = ($I_{OLED_ON} \cdot t_{ON} + I_{OLED_OFF} \cdot t_{OFF}$) / ($t_{ON} + t_{OFF}$), where t_{ON} and t_{OFF} is the ON- and OFF-period during the frame time, respectively. The variation of I_{AVE} versus I_{DATA} in one frame period ($t_{ON} + t_{OFF}$) for different C_{ST2}/C_{ST1} ratios is shown in Fig. 2 (c). Since the OFF-state period is much longer than ON-state, though I_{OLED_OFF} is very small during OFF-state, it can reduce the I_{AVE} even if the I_{OLED_ON} (= I_{DATA}) is large. For example, the pixel electrode circuit can generate I_{AVE} ranging from 2.3 nA to 2.5 μ A while I_{DATA} swept from 0.2 to 5 μ A. Therefore, during one frame time, we can achieve very wide range of OLED current levels by supplying high data current levels.

The evolution of the scaling ratio (R_{SCALE}=



Figure 3 Variation of the current scaling ratio as a function of (a) I_{DATA} and (b) ratio of storage capacitances for the proposed pixel circuit.

 I_{OLED_ON}/I_{OLED_OFF}) for different ratios of C_{ST2}/C_{ST1} as a function of I_{DATA} is shown in Fig. 3 (a). In this figure, we can see that for $C_{ST2}/C_{ST1}=1/6$, R_{SCALE} decreases from 14303 to 2.0 as I_{DATA} increases from 0.2 to 5µA, and an ideal non-linearity of R_{SCALE} can be achieved; e.g. a very high R_{SCALE} at low I_{DATA} levels (low gray scales) and a low R_{SCALE} at high I_{DATA} levels (high gray scales) can be produced. The variation of R_{SCALE} with the C_{ST2}/C_{ST1} is also shown in Fig. 3 (b). The simulated results show that for fixed I_{DATA} , R_{SCALE} increases as C_{ST2} increase from 30 to 90 fF, corresponding to an increase of C_{ST2}/C_{ST1} from 1/12 to 1/4. For constant C_{ST2}/C_{ST1} , R_{SCALE} increases as I_{DATA} decreases as shown in Fig. 3 (a). Therefore, for a fixed ratio of C_{ST2}/C_{ST1} determined from the pixel electrode circuit design, we can

4. Comparison with Other Pixel Electrode Circuits

To demonstrate the current-scaling function of the pixel electrode circuit in comparison with both the conventional



current-mirror [5] and cascade capacitor current-scaling pixel electrode circuits [4], we simulated all three pixel electrode circuits using H-SPICE, and measured IOLED OFF as a function of IDATA for each pixel electrode circuit as shown in Fig. 4. While the conventional current-mirror pixel circuit showed only a fixed current-scaling by the ratio of T4/T3 over all IDATA range, the cascade capacitor current-scaling and the proposed current-scaling pixel electrode circuits showed non-linear current-scaling function for variable current-scaling ratio depending on IDATA. When IDATA varies from 0.2 to 5.0 µA, the proposed cascaded-capacitor pixel circuit with the ratio of $C_{ST2}/C_{ST1}=1/6$ can provide $I_{OLED OFF}$ ranging from 1.7×10^{-5} to 2.5 µA. Hence much wider range I_{OLED OFF} levels can be achieved by this circuit in comparison with the conventional current-mirror pixel circuit $(3.0 \times 10^{-2}$ to 1.0 µA). And slightly wider range is obtained in comparison with the cascade capacitor currentscaling pixel circuit (8.8×10⁻⁵ to 2.0 $\mu A).$ It should be noted that though the I_{OLED OFF} curve of proposed circuit is steeper than cascade capacitor circuit in Fig. 4, its shape can be adjusted to the required gray levels by controlling device parameters.

5. Conclusion

When a low I_{DATA} is used to express a low gray scale, the conventional current-driven pixel circuit has a problem of slow programming time. On the contrary, when a high I_{DATA}

is used to express a high gray scale, the current-mirror circuit has a problem of high power consumption due to a fixed current-scaling ratio. On the contrary, the cascadecapacitor circuit provides the comparable non-linear currentscaling to the proposed circuit but needs an additional control signal line which could complicate the pixel layout and driving scheme. In the proposed circuit, by employing the cascaded-capacitors connected to the driving TFT, we could produce better non-linear scaling-function than the cascade capacitor circuit, which has a high scaling ratio at low current levels and a low scaling ratio at high current levels. Therefore, using this pixel circuit, we expect to avoid the unnecessary pixel circuit power consumption at high current levels and minimize the programming time at low current levels with reduced number of signal lines, which are supposed to be ideal characteristics for a high-resolution AM-OLED based on a-Si:H TFTs.

6. Acknowledgements

This work was supported by LG Philips LCD Research & Development Center, Korea.

7. References

1) Y. He, R. Hattori, and J. Kanicki, IEEE Trans. Electron Devices, vol. 48, p.1322, 2001.

T. V. de Biggelaar, I. Camps, M. Childs, M. Fleuster, A. Giraldo,
S. Godfrey, I. M. Hunter, M. T. Johnson, H. Lifka, R. Los, A. Sempel, J. M. Shannon, M. J. Trainor, R. W. Wilks, and N. D. Young, Proceedings of SPIE, vol. 4295, p.134, 2001.

3) Y. Hong, J. Y. Nam, and J. Kanicki, IEEE J. Selected Topics in Quantum Electron., vol. 10, p.16, 2004.

4) Y. C. Lin, H. P. D. Shieh, and J. Kanicki, IEEE Trans. Electron Devices, vol. 52, p.1123, 2005.

5) A. Yumoto, M. Asano, H. Hasegawa, and M. Sekiya, in Proc. Int. Display Workshop, p.1395, 2001.

6) J. Lee, W. Nam, S. Jung, and M. Han, IEEE Electron Device Lett., vol. 25, p.280, 2004.

7) J. Lee, W. Nam, S. Han, and M. Han, SID 03 Digest, p. 490, 2003.